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TITLE OF THE INVENTION

METHOD AND SYSTEM FOR MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method and system for manufacturing a semiconductor device. More particularly, the present invention relates to a manufacturing method and system effective for increasing the yield of a semiconductor device.

2. Description of the Background Art

There has hitherto been proposed a technique of stabilizing processes by means of measuring the thickness of a film formed on a wafer before and after etching, and feeding back a measurement result to etching requirements. For instance, Japanese Patent Application Laid-Open No. H10-275753 describes a technique of measuring the thickness of a film at an arbitrary frequency after formation or etching of a predetermined film, thus ascertaining successive variations in a film-growth system and an etching system on the basis of the result of measurement. In the related art technique, information pertaining to the thus-ascertained successive variations is utilized as basic data to be used for determining the time at which an alarm is to be issued or the time at which maintenance of the system is to be performed, or as basic data to be used for adjusting film-growth requirements or etching requirements. Japanese Patent Application Laid-Open No. H7-29958 describes a technique of performing predetermined inspection before and after processing of a wafer, thereby automatically changing wafer processing requirements on the basis of an inspection result.

These related-art techniques are to feed back the result of inspection of a wafer before and after predetermined processing to requirements for the processing. In short, the related-art techniques are to correct processing requirements for a certain

process, in accordance with the state of the wafer which has been subjected to the process. In this case, the result of inspection of a certain wafer is not reflected in the processing of the wafer. In this respect, the related-art techniques encounter a problem of processing errors of respective processes being accumulated in respective wafers.

SUMMARY OF THE INVENTION

The present invention has been conceived to solve such a problem and is aimed at providing a manufacturing method which enables high-yield manufacture of a semiconductor device of stable quality, by means of reflecting the state of a wafer in the requirements for processing the wafer through use of the feedforward technique.

The present invention is also aimed at providing a manufacturing system which enables high-yield manufacture of a semiconductor device of stable quality, by means of reflecting the state of a wafer in requirements for processing the wafer through use of the feedforward technique.

The above objects of the present invention are achieved by a method of manufacturing a semiconductor device described below. The method includes a first step of acquiring a measurement value pertaining to a wafer to be subjected to a predetermined processing process. The method also includes a second step of determining processing requirements for the predetermined processing process on the basis of the measurement value. The method further includes third step of performing the predetermined processing process in accordance with the processing requirements determined in the second step.

The above objects of the present invention are achieved by a method of manufacturing a semiconductor device described below. The method includes a step of wet etching a predetermined film to be processed. The method also includes a step of counting

a time which has elapsed since replacement of a chemical to be used for the wet etching. The method further includes a step of determining processing requirements for the wet etching on the basis of the elapsed time. The wet etching is performed in accordance with the processing requirements.

The above objects of the present invention are achieved by a semiconductor device manufacturing system which performs a plurality of processing processes. The system includes a measurement apparatus for acquiring a predetermined measurement value pertaining to a wafer to be subjected to a predetermined processing process. The system also includes a recipe determination section for determining processing requirements for the predetermined processing process on the basis of the measurement value. The system further includes a processing apparatus for performing the predetermined processing process in accordance with the processing requirements determined by the recipe determination section.

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram for describing a construction of a system for manufacturing a semiconductor device according to a first embodiment of the present invention;

Fig. 2A is a cross sectional view for describing a manufacturing method according to the first embodiment of the present invention;

Fig. 2B is a flowchart for describing a manufacturing method according to the first embodiment of the present invention;

Fig. 3A is a cross sectional view for describing a manufacturing method according to a second embodiment of the present invention;

Fig. 3B is a flowchart for describing a manufacturing method according to a second embodiment of the present invention;

Fig. 4A is a cross sectional view for describing a manufacturing method according to a third embodiment of the present invention;

Fig. 4B is a flowchart for describing a manufacturing method according to a third embodiment of the present invention;

Fig. 5A is a cross sectional view for describing a manufacturing method according to a forth embodiment of the present invention;

Fig. 5B is a flowchart for describing a manufacturing method according to a fourth embodiment of the present invention;

Fig. 6 is a graph showing a relationship between an etching rate and an impurity concentration;

Figs. 7A through 7D are cross sectional views for describing a manufacturing method according to a fifth embodiment of the present invention;

Fig. 7E is a flowchart for describing a manufacturing method according to a fifth embodiment of the present invention; and

Fig. 8 is a block diagram for describing a construction of a system for manufacturing a semiconductor device according to a sixth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described by reference to the accompanying drawings. Throughout the drawings, like elements are assigned like reference numerals, and repetition of their explanations is omitted.

First Embodiment

Fig. 1 is a block diagram showing the construction of a system for manufacturing a semiconductor device according to a first embodiment of the present invention. As shown in Fig. 1, the manufacturing system according to the present embodiment

comprises a main computer 10, a measurement apparatus 12, and a processing apparatus 14. The main computer 10, the measurement apparatus 12, and the processing apparatus 14 are interconnected by way of a communications channel so as to effect mutual communication of information.

The processing apparatus 14 is to perform various processing operations to be performed during the course of manufacture of a semiconductor device. The processing apparatus 14 is constituted of, for example, a film-growth machine for forming a predetermined film on a wafer, and a dry or wet etching machine for etching the film formed on the wafer. Although a plurality of pieces of processing apparatus 14 are shown in Fig. 1, the manufacturing system according to the present embodiment may comprise only one processing apparatus 14.

The measurement apparatus 12 is to subject a wafer to a predetermined inspection during the course of manufacture of a semiconductor device. The measurement apparatus 12 is constituted of, for example, a film thickness measurement machine for measuring the thickness of a film formed on the surface of a wafer; an impurity measurement machine for measuring the concentration of impurities contained in the film formed on the surface of the wafer; a size measurement machine for measuring the size of a pattern formed on the surface of a wafer; or an interlayer oxide film measurement machine for measuring an interlayer oxide film formed on the surface of the wafer. Although Fig. 1 shows only one measurement machine 12, a plurality of measurement machines 12 may be provided within the manufacturing system according to the present embodiment.

The main computer 10 is equipped with a measurement value receiving section 16 for receiving a value measured by the measurement apparatus 12. The measurement value received by the measurement value receiving section 16 is stored into measurement value memory 20 along with an ID assigned to a wafer which is

an object of measurement, by means of a measurement value memorizing section 18.

The main computer 10 is also equipped with an ID receiving section 22. Before starting processing of a wafer, the processing apparatus 14 sends to the main computer 10 the ID assigned to a wafer which is an object of processing. Hereinafter, the processing apparatus 14 that has transmitted an ID will be referred to specifically as an "object-of-control processing apparatus 14." The ID receiving section 22 receives the ID transmitted by the object-of-control processing apparatus 14 and transfers the thus-received ID to a recipe determination section. In accordance with the ID, the recipe determination section 24 reads from the measurement value memory 20 the measurement value pertaining to the wafer to be processed by the object-of-control processing apparatus 14; more particularly, a measurement value measured immediately before the object-of-control processing apparatus 14 performs processing.

Requirements which are used by the object-of-control processing apparatus 14 to process a wafer should be set appropriately in accordance with the state of the wafer at a point in time at which the processing is commenced. More specifically, the requirements which are used by the object-of-control processing apparatus 14 to process a wafer should be set appropriately in accordance with a measured value pertaining to the wafer measured immediately before the processing.

A recipe memory 26 provided to the main computer 10 stores optimal processing requirements for the object-of-control processing apparatus 14 that have been determined beforehand on the basis of a relation with the above mentioned measured value. The recipe determination section 24 described above reads out a measured value from the measurement value memory 20 so as to reads out optimal processing requirements from the recipe memory 26 based on the measured value. The thus-read optimal processing

requirements are sent to the object-of-control processing apparatus 14 by means of a recipe transmission section 28.

The object-of-control processing apparatus 14 processes the wafer according to the optimal requirements thus transmitted from the main computer 10. As mentioned above, the manufacturing system according to the present embodiment can reflect the state of the wafer measured by the measurement apparatus 12 in the processing requirements for the object-of-control processing apparatus 14, by means of the feedforward technique. More specifically, the manufacturing system according to the present embodiment can reflect the state of a wafer measured by the measurement apparatus 12 in requirements used for processing the wafer itself. Therefore, the manufacturing system according to the present embodiment enables high-yield manufacture of a semiconductor device of stable quality without errors of respective processes being accumulated in a wafer.

The operation of the manufacturing system according to the first embodiment of the present invention will be described in more detail by reference to Figs. 2A and 2B.

The manufacturing system according to the present embodiment is aimed at accurately controlling a step difference between the surface of an isolation oxide film to be embedded in a trench and the surface of a silicon substrate, during the course of manufacture of an element isolation structure through use of a trench structure. During the course of manufacture of an element isolation structure using a trench isolation structure, processing described below is performed.

As shown in Fig. 2A, a silicon oxide film 35, a polysilicon film 34, and a silicon nitride film 32 are formed on the surface of a silicon substrate 31. The silicon nitride film 32 is patterned in accordance with the geometry of a trench to be formed. The silicon substrate 31 is subjected to dry etching while the thus-patterned silicon nitride film 32 is used as a mask, whereby

a trench structure is formed in the silicon substrate 31. An oxide film is deposited on the entire surface of the silicon substrate 31 such that the trench structure is filled with the oxide film, by means of chemical vapor deposition (CVD). Subsequently, the oxide film overflowing the trench structure is removed by means of chemical-and-mechanical polishing (CMP), to thereby remain the oxide film within only the trench structure for forming an isolation oxide film 33.

In the present embodiment, CMP is followed by etching of the isolation oxide film 33, etching of the silicon nitride film 32, and etching of the polysilicon film 34, in the sequence given. During the course of the previously-described round of processing, comparatively large errors are likely to arise in the abrasion amount to be attained in the course of CMP. For this reason, if etching of the isolation oxide film 33 is performed in accordance with default requirements, difficult is encountered in accurately forming a step difference between the surface of the isolation oxide film 33 and the surface of the silicon substrate 31 such that the step assumes a desired final value.

As shown in Fig. 2B, in the present embodiment, after CMP processing of the oxide film has been completed, the thickness of the isolation oxide film 33 is measured. The resultant measurement value is reflected in the requirements for etching the isolation oxide film 33, by means of the feedforward technique. In the present embodiment, a film thickness measurement apparatus used for measuring the thickness of the isolation oxide film 33 after CMP corresponds to the measurement apparatus 12 shown in Fig. 1. Further, an etching machine used for etching the isolation oxide film 33 corresponds to the object-of-control processing apparatus 14.

Every time CMP of a wafer is completed, the manufacturing system according to the embodiment measures the thickness of the isolation oxide film 33 formed on the wafer. The resultant

measurement value is transmitted to the main computer 10, and the thus-transmitted measurement value is recorded in the measurement value memory 20 along with the ID assigned to the wafer. Further, when the wafer has reached a process of etching the isolation oxide film 33, the etching machine requests the main computer 10 to transmit optimal requirements. Thus, processing requirements for the etching machine are set to the optimal requirements determined by the recipe determination section 24. Subsequently, the isolation oxide film 33 is etched according to the optimal requirements.

The manufacturing method according to the present embodiment enables a step difference between the surface of the isolation oxide film 33 and the surface of the silicon substrate 31 to be accurately controlled to a desired value at all times finally, regardless of variations in the amount of abrasion attained in the course of CMP. Accordingly, the manufacturing method and system according to the present embodiment enable high-yield manufacture of a semiconductor device of stable quality.

In the first embodiment, an ID is set on a per-wafer basis, and requirements for etching the isolation oxide film 33 are set on a per-wafer basis. The present invention is not limited to this embodiment. Specifically, an ID may be set on a per-lot basis, and etching requirements may be set on a per-lot basis.

In the first embodiment, processing requirements are set within the main computer 10, and the requirements are sent from the main computer 10 to the etching apparatus (the object-of-control apparatus 14). The present invention is not limited to this embodiment. Specifically, a plurality of processing requirements may be stored beforehand in the etching machine, and the main computer 10 may select optimal requirements from the requirements.

Second Embodiment

A second embodiment of the present invention will now be described by reference to Figs. 3A and 3B.

Under the manufacturing method according to the present embodiment, after a wafer has been subjected to CMP in accordance with the same procedures as those employed in the first embodiment, the silicon nitride film 32 is etched, as shown in Fig. 3B. Fig. 3A shows the wafer in which the silicon nitride film 32 has been removed from the polysilicon film 34.

After etching of the silicon nitride film 32, the measurement apparatus 12 measures the thickness of the isolation oxide film 33. The thus-measured thickness value is transmitted to the main computer 10 in the same manner as in the first embodiment, and the value is recorded along with an ID assigned to the wafer.

The isolation oxide film 33 is etched from the wafer. At this time, processing requirements for the etching machine (corresponding to the object-of-control processing apparatus 14) are set to optimal requirements by the main computer 10, as in the case of the first embodiment.

By means of the manufacturing method and system according to the present embodiment, variations in the thickness of the isolation oxide film 33 stemming from CMP and variations in the thickness of the isolation oxide film stemming from removal of the silicon nitride film 32 can be reflected in the requirements for etching the isolation oxide film 33. The manufacturing method and system according to the present embodiment enable more accurate control of the step between the surface of the isolation oxide film 33 and the surface of the silicon substrate 31 to a desired value than that attained in the first embodiment.

Third Embodiment

A third embodiment of the present invention will now be described by reference to Figs. 4A and 4B.

The third embodiment is aimed at accurately controlling the thickness of an interlayer oxide film during an etching process

intended for smoothing the interlayer oxide film of a semiconductor device. In the present embodiment, processing is effected in the following manner during the course of manufacture of a semiconductor device.

As shown in Fig. 4A, various interconnection elements such as a gate electrode 38 of a transistor and a capacitor electrode 40 of a memory cell are formed on the silicon substrate 31. An interconnection oxide film 42 is deposited on the entire surface of the silicon substrate 31 so as to cover all the interconnection elements, by means of, for example, the CVD technique. At this time, on the surface of the interlayer oxide film 42 there are formed steps difference ascribable to presence/absence of the interconnection elements and structural dissimilarities between the interconnection elements.

In a subsequent process, an unillustrated upper interconnection is formed on the interlayer oxide film 42. The step differences formed on the surface of the interlayer oxide film 42 would induce patterning failures at the time of formation of an upper interconnection. For this reason, in the present embodiment, a resist film 44 is formed so as to cover recessed areas of the interlayer oxide film 42, then the interlayer oxide film 42 is etched back while the resist film 44 is taken as a mask, before formation of an upper interconnection.

As shown in Fig. 4B, in the present embodiment, after the interlayer oxide film 42 has been deposited, the thickness of the interlayer oxide film 42 is measured before a resist film 44 is formed by means of photolithography. The resultantly-measured value is reflected in the requirements for etching back the interlayer oxide film 42, by means of the feedforward technique. In the present embodiment, a film thickness measurement apparatus for measuring the thickness of the interlayer oxide film 42 after deposition thereof corresponds to the measurement apparatus 12 shown in Fig. 1. Further, an

etching machine used for etching back the interlayer oxide film 42 corresponds to the object-of-control processing apparatus 14.

By means of the manufacturing system according to the present embodiment, a film thickness measurement apparatus (corresponding to the measurement apparatus 12) measures the thickness of the interlayer oxide film 42 immediately after deposition thereof on a wafer. The resultantly-measured value is transmitted to the main computer 10, and the value is recorded in the measurement value memory 20 along with an ID assigned to the thus-measured wafer. When the wafer has reached a process of etching back the interlayer oxide film 42, the etching machine (corresponding to the object-of-control apparatus 14) requests the main computer 10 to transmit optimal requirements. The recipe determination section 24 of the main computer 10 sets as processing requirements for the etching machine the optimal requirements, which are determined on the basis of the thickness of the interlayer oxide film 42.

According to the manufacturing method, the thickness of the interlayer oxide film 42 can be made uniform to high accuracy before formation of an upper interconnection. The manufacturing method and system according to the present embodiment enable effective prevention of patterning failures in an upper interconnection and high-yield manufacture of a semiconductor device of stable quality.

In the third embodiment, an ID is set on a per-wafer basis, and requirements for etching the interlayer oxide film 42 are also set on a per-wafer basis. However, the present invention is not limited to this embodiment. Specifically, an ID may be set on a per-lot basis, and etching requirements may be set on a per-lot basis.

In the third embodiment, processing requirements are set within the main computer 10, and the thus-set processing requirements are transmitted from the main computer 10 to the

etching machine (corresponding to the object-of-control processing machine 14). However, the present invention is not limited to this embodiment. More specifically, a plurality of processing requirements may be stored beforehand in the etching machine, and the main computer 10 may select optimal requirements from the requirements.

Fourth Embodiment

A fourth embodiment of the present invention will now be described by reference to Figs. 5A and 5B.

The present embodiment is aimed at accurately controlling the thickness of an interlayer oxide film during an etching process intended for smoothing the interlayer oxide film of a semiconductor device, as in the case of the third embodiment. The following description pertains to the difference between the third and fourth embodiments.

In the present embodiment, an oxide film containing impurities, such as B or P, is used for the interlayer oxide film 42. In a case where the interlayer oxide film 42 is formed from an oxide film containing B or P, ease of smoothing can be enhanced. Accordingly, under the manufacturing method according to the present embodiment, the interlayer oxide film 42 can be smoothed more readily than in the third embodiment.

In a case where the interlayer oxide film 42 is doped with impurities, the concentration of impurities affects the rate at which the interlayer oxide film 42 is etched. Fig. 6 is a graph showing the influence of the concentration of P in an oxide film on a rate at which the oxide film is etched, during a wet etching operation using buffered hydrofluoric acid (i.e., a mixture consisting of HF_4F and HF). As shown in Fig. 6, the rate at which an oxide film is etched increases with an increase in the concentration of P. Accordingly, the concentration of impurities contained in the interlayer oxide film 42 is one of

the primary factors determining the thickness of the interlayer oxide film 42 still remaining after the etching process.

As shown in Fig. 5B, in the present embodiment, the concentration of impurities contained in the interlayer oxide film 42 is measured after deposition of the interlayer oxide film 42 and before the formation of the resist film 44 by means of photolithography. The resultantly-measured value is reflected in the requirements for etching back the interlayer oxide film 42, by means of the feedforward technique. In the present embodiment, an impurity concentration measurement apparatus used for measuring the concentration of impurities contained in the interlayer oxide film 42 after deposition thereof corresponds to the measurement apparatus 12 shown in Fig. 1. Further, the etching machine used for etching back the interlayer oxide film 42 corresponds to the object-of-control processing apparatus 14.

The manufacturing system according to the present embodiment measures the concentration of impurities contained in the interlayer oxide film 42 using the impurity measurement apparatus (i.e., the measurement apparatus 12) immediately after the interlayer oxide film 42 is deposited on the wafer. The resultantly-measured value is transmitted to the main computer 10, and the value is recorded in the measurement value memory 20 along with the ID assigned to the thus-measured wafer. When the wafer has reached a process of etching back the interlayer oxide film 42, the etching machine (i.e., the object-of-control processing apparatus 14) requests the main computer 10 to transmit optimal requirements. The recipe determination section 24 of the main computer 10 sets as processing requirements for the etching machine the optimal requirements, which are determined on the basis of the concentration of impurity in the interlayer oxide film 42. Subsequently, the interlayer oxide film 42 is etched back under the optimal requirements.

According to the manufacturing method, the thickness of the interlayer oxide film 42 can be made uniform to high accuracy before formation of an upper interconnection. The manufacturing method and system according to the present embodiment enable prevention of patterning failures in an upper interconnection, and high-yield manufacture of a semiconductor device of stable quality.

In the fourth embodiment, an ID is set on a per-wafer basis, and requirements for etching the interlayer oxide film 42 are also set on a per-wafer basis. However, the present invention is not limited to this embodiment. Specifically, an ID may be set on a per-lot basis, and etching requirements may be set on a per-lot basis.

In the fourth embodiment, processing requirements are set within the main computer 10, and the thus-set processing requirements are transmitted from the main computer 10 to the etching machine (corresponding to the object-of-control processing machine 14). However, the present invention is not limited to this embodiment. More specifically, a plurality of processing requirements may be stored beforehand in the etching machine, and the main computer 10 may select optimal requirements from the requirements.

In the first through third embodiments set forth, the requirements for etching the isolation oxide film 33 or the interlayer oxide film 42 are determined on the basis of the thickness of the isolation oxide film 33 or the interlayer oxide film 42. In the fourth embodiment, the requirements for etching the interlayer oxide film 42 are determined on the basis of the concentration of impurities contained in the interlayer oxide film 42. However, data used for determining the requirements for etching the isolation oxide film 33 or the interlayer oxide film 42 are not limited to the film thickness or the concentration of impurities. For instance, the requirements for etching the

isolation oxide film 33 or the interlayer oxide film 42 may be determined on the basis of the refractive index of the films.

Fifth Embodiment

A fifth embodiment of the present invention will now be described by reference to Figs. 7A through 7E.

The fifth embodiment is aimed at accurate formation of a miniaturized interconnection pattern. In the present embodiment, the processing described below is performed during the course of manufacture of a semiconductor device.

As shown in Fig. 7A, an interconnection layer 46 and an oxide film 48 are formed on the silicon substrate 31. The interconnection layer 46 is formed from, for example, doped polysilicon or metal material such as tungsten or tungsten silicide. A resist film 50 which is slightly larger than a miniaturized pattern to be formed is patterned on the oxide film 48 by means of photolithography.

The oxide film 48 is dry-etched while the resist film 50 is taken as a mask. Subsequently, the resist film 50 still remaining on the oxide film 48 is removed by means of oxygen plasma processing. As a result, there is formed the wafer, as shown in Fig. 7B.

As shown in Fig. 7C, the outer dimension of the oxide film 48 is reduced by means of wet etching. The oxide film 48 thus reduced turns into a miniaturized pattern which cannot be formed by means of dry etching.

As shown in Fig. 7D, the interconnection layer 46 is dry-etched while the reduced oxide film 48 is taken as a mask. Consequently, an interconnection 52 having a miniaturized pattern is formed on the silicon substrate 31.

The principal reasons for causing dimensional errors in the interconnection 52 formed through the foregoing procedures are (1) dimensional errors in the resist film 50 formed by means of photolithography and (2) dimensional errors in the oxide film

48 caused by side etching, which etching would arise during the dry etching process. In the present embodiment, in order to accurately set the final dimension of the interconnection 52 to a desired value, dimensional errors in the resist film 50 and those in the oxide film 48 are corrected by means of the technique to be described below.

As shown in Fig. 7E, in the present embodiment, the resist film 50 is formed through use of photolithography at first. Then, the oxide film 48 is dry-etched using the resist film 50 as a mask. After removing the resist film 50, the dimension of the patterned oxide film 48 is measured. The resultantly-measured value is reflected in the requirements for wet-etching the oxide film 48 by means of the feedforward technique. In the present embodiment, the dimension measurement apparatus used for measuring the dimension of the oxide film 12 after removal of the resist film 50 corresponds to the measurement apparatus 12. Further, the wet-etching apparatus used for wet-etching the oxide film 12 corresponds to the object-of-control processing apparatus 14.

The manufacturing system according to the present embodiment measures the dimension of the oxide film 48 using the dimension measurement apparatus (i.e., the measurement apparatus 12) before the oxide film 48 is subjected to wet etching. The resultantly-measured value is transmitted to the main computer 10, and the value is recorded in the measurement value memory 20 along with the ID assigned to the thus-measured wafer. In addition, when the wafer has reached a wet-etching process, the wet etching apparatus (i.e., the object-of-control processing apparatus 14) requests the main computer 10 to transmit optimal requirements. The recipe determination section 24 of the main computer 10 sets the optimal requirements, which are determined on the basis of the dimension of the oxide film 48, as processing

requirements for the etching machine. Subsequently, the oxide film 48 is wet-etched under the optimal requirements.

According to the manufacturing method set forth, dimensional errors in the resist film 50 or dimensional errors in the oxide film 48 stemming from side etching can be absorbed by wet etching. For this reason, the manufacturing method and system according to the present embodiment enable considerably-accurate patterning of a minute interconnection 52 and high-yield manufacture of a semiconductor device of stable quality.

In the fifth embodiment, an ID is set on a per-wafer basis, and requirements for etching the oxide film 12 are also set on a per-wafer basis. However, the present invention is not limited to this embodiment. Specifically, an ID may be set on a per-lot basis, and etching requirements may be set on a per-lot basis.

In the fifth embodiment, processing requirements are set within the main computer 10, and the thus-set processing requirements are transmitted from the main computer 10 to the etching machine (corresponding to the object-of-control processing machine 14). However, the present invention is not limited to this embodiment. More specifically, a plurality of processing requirements may be stored beforehand in the etching machine, and the main computer 10 may select optimal requirements from the requirements.

Sixth Embodiment

A sixth embodiment of the present invention will now be described by reference to Fig. 8.

Fig. 8 is a block diagram for describing the characteristic part of the manufacturing system according to the present embodiment. In addition to the manufacturing system described in connection with the fifth embodiment, the manufacturing system according to the present embodiment further comprises a recipe correction section 54 and an elapsed-time management section 56.

The recipe correction section 54 and the elapsed-time management section 56 can be disposed within the main computer 10 or within the wet etching machine (i.e., within the processing apparatus 14).

The elapsed-time management section 56 is a unit for counting the time which has elapsed since replacement of a chemical stored in the wet etching machine with a fresh chemical. The recipe correction section 54 is a unit for correcting the basic recipe for wet etching in accordance with the elapsed time. A wet etching chemical deteriorates with elapse of time. In addition, an etch rate of wet etching changes in accordance with the deterioration of the chemical. Therefore, it is effective for accurately etching the oxide film 48 by means of wet etching to correct wet-etching requirements in accordance with the time which has elapsed since replacement of the chemical.

In the manufacturing system according to the present embodiment, wet-etching requirements can be corrected on the basis of the dimension of the oxide film 48 which has been dry-etched. Further, wet-etching requirements can be corrected in accordance with the time which has elapsed since replacement of a chemical. The manufacturing system and method according to the present embodiment enables the interconnection 52 to be patterned more accurately than in the fifth embodiment.

The sixth embodiment employs two techniques in combination; that is, the technique of reflecting the dimension of the dry-etched oxide film 48 in the requirements for wet etching the oxide film 48, by means of the feedforward technique; and the technique of reflecting the time which has elapsed since replacement of the chemical in the wet-etching requirements. The present invention is not limited to this embodiment. More specifically, the technique of correcting the wet-etching requirements in accordance with the time which has elapsed since replacement of the chemical may be used solely in isolation from

the technique of correcting the wet-etching requirements in accordance with the dimension of the oxide film 48.

In the first through sixth embodiments, requirements for only etching (either dry etching or wet etching) are corrected by means of the feedforward technique. Processing which may be corrected by means of the feedforward technique is not limited to the above-described technique. For instance, film-growth requirements or CMP requirements may be corrected by means of the feedforward technique.

The present invention which has been embodied in the manner as mentioned previously yields the following effects.

According to a first aspect of the present invention, the state of a wafer which is an object of processing can be reflected in the requirements for processing the wafer, by means of the feedforward technique. Hence, the present invention enables high-yield manufacture of a semiconductor device of stable quality.

According to a second aspect of the present invention, the physical quantity of a film to be processed can be reflected in the requirements for etching the film. Accordingly, the present invention enables accurate etching of the film.

According to a third aspect of the present invention, the thickness of a film to be processed can be reflected in etching requirements. Accordingly, the present invention enables accurate etching of the film without regard to variations in the thickness of the film.

According to a fourth aspect of the present invention, the concentration of impurities contained in a film to be processed can be reflected in etching requirements. Hence, the present invention enables accurate etching of the film without regard to a difference in etch rate due to a difference in concentration of impurities.

According to a fifth aspect of the present invention, the refractive index of a film to be processed can be reflected in etching requirements. The present invention enables accurate etching of the film without regard to a difference in etch rate due to a difference in refractive index.

According to a sixth aspect of the present invention, the dimension of a film to be processed can be reflected in etching requirements. The present invention enables accurate miniaturization of a film to a desired dimension without regard to the dimension of the film at a point in time at which etching of the film is commenced.

According to a seventh aspect of the present invention, processing requirements according with a measurement value are determined within the main computer, and the processing requirements can be set in a processing apparatus.

According to a eighth aspect of the present invention, processing requirements according with a measurement value can be determined within a processing apparatus.

According to a ninth aspect of the present invention, wet-etching requirements can be corrected in accordance with the state of a chemical. Therefore, the present invention enables accurate wet-etching of a film to be processed at all times, without regard to deterioration of the chemical.

Further, the present invention is not limited to these embodiments, but variations and modifications may be made without departing from the scope of the present invention.

The entire disclosure of Japanese Patent Application No. 2000-349027 filed on November 16, 2000 including specification, claims, drawings and summary are incorporated herein by reference in its entirety.